AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of manufacturing a semiconductor device comprising:

(a) a first wiring extending in a first direction; and

(b) a second wiring connected to the first wiring through a connection and extending in a second direction orthogonal to the first direction, the second wiring having a surplus portion projecting from the connection in a direction opposite to the second direction,

wherein the first wiring and the second wiring are arranged such that,

(c) a center of the connection is offset in the second direction from a center of the first wiring, and

(d) a projecting portion of the first wiring is disposed under the connection.

2. (Previously Presented) A method of manufacturing a semiconductor device, comprising:

(a) a first wiring and a second wiring extending in a first direction and being adjacent to each other;

(b) a third wiring connected to the first wiring through a first connection and extending in a direction opposite to the second wiring and along a line orthogonal to the first direction, the third wiring having a first surplus portion projecting in the direction of the second wiring from the first connection; and

(c) a fourth wiring connected to the second wiring through a second connection and extending along said line in a direction opposite to the first wiring, the fourth wiring having a second surplus portion projecting in the direction of the first wiring from the second connection,

wherein the first, second, third, and fourth wirings are arranged such that,

(d) a center of the second connection is offset in a direction opposite to the first wiring from a center of the second wiring, and

(e) a projecting portion of the second wiring is disposed under the second connection.

3. (original) The method according to claim 2, wherein the spacing between a center of the first wiring and that of the second wiring is a unit distance in wiring.

4. (original) The method according to claim 2, wherein a fifth wiring is disposed in parallel with the third wiring.

5. (original) The method according to claim 4, wherein the distance between the third and the fifth wirings is smaller than the distance between the first and the second wirings.

6. (original) The method according to claim 4 or claim 5, wherein the distance between the first and the second wirings is larger than a minimum machining size.

7. (Previously Presented) The method according to claim 4 or claim 5, wherein the width of each of the first and the second surplus portions is smaller than the difference (P0-P1) between a distance P1 between a center of the third wiring

and that of the fifth wiring and a distance P0 between a center of the first wiring and that of the second wiring, and is larger than one half of the difference between the distances P1 and P0.

8. (currently amended) The method according to claim 2, wherein the width of each of the first wiring and the second wiring and the width of each of the first connection and the second connection are ~~almost~~ substantially equal to each other.

9. (original) The method according to claim 2,

wherein a MISFET underlies the first and the second wirings, and

wherein a gate electrode of the MISFET is disposed in the first direction between the first and the second wirings.

10. (original) The method according to claim 2,

wherein a MISFET underlies the first and the second wirings, and

wherein the first or the second wiring is connected to a source and a drain, or a gate electrode, of the MISFET.

11. (original) The method according to claim 2, wherein a center of the first connection is disposed on a center of the first wiring.

12. (original) The method according to claim 2,

(f) wherein a center of the first connection is offset from a center of the first wiring in a direction opposite to the second wiring, and

(g) wherein a projecting portion of the first wiring is disposed under the first connection.

13. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) disposing a first wiring and a second wiring extending in a first direction and being adjacent to each other;

(b) disposing a third wiring being connected to the first wiring through a first connection and extending in a second direction orthogonal to the first direction and in opposition to the second wiring, the third wiring having a first surplus portion projecting in the direction of the second wiring from the first connection;

(c) disposing a fourth wiring being connected to the second wiring through a second connection and extending in the second direction and in opposition to the first wiring, the fourth wiring having a second surplus portion projecting in the direction of the first wiring from the second connection;

(d) determining whether the third wiring and the fourth wiring are positioned on ~~one and~~ the same line and whether the distance between the first and the second surplus portions is a predetermined distance or less;

(e) if the distance between the first and the second surplus portions is the predetermined distance or less,

displacing a center of the second connection from a center of the second wiring in a direction opposite to the first wiring; and

(f) disposing a projecting portion of the second wiring under the second connection.

14. (original) The method according to claim 13, wherein the spacing between a center of the first wiring and that of the second wiring is a unit distance in wiring.

15. (original) The method according to claim 13, wherein a fifth wiring is disposed in parallel with the third wiring.

16. (original) The method according to claim 16, wherein the distance between the third and the fifth wirings is smaller than the distance between the first and the second wirings.

17. (original) The method according to claim 15, wherein the distance between the first and the second wirings is larger than a minimum machining size.

18. (original) The method according to any of claims 15 to 17, wherein the width of each of the first and the second surplus portions is smaller than the difference (P0-P1) between a distance P1 between a center of the third wiring and that of the fifth wiring and a distance P0 between a center of the first wiring and that of the second wiring, and is larger than one half of the difference between the distances P1 and P0.

19. (Currently Amended) The method according to claim 13, wherein the width of each of the first and the second wirings and the width of each of the first and the second connections are ~~almost~~ substantially equal to each other.

20. (original) The method according to claim 13,

wherein a MISFET underlies the first and the second wirings, and

wherein a gate electrode of the MISFET is disposed in the first direction between the first and the second wirings.

21. (Previously Presented) The method according to any of claims 13 to 20,

wherein a MISFET underlies the first and the second wirings, and

wherein the first wiring or the second wiring is connected to a source and a drain, or a gate electrode, of the MISFET.

22. (original) The method according to claim 13, wherein a center of the first connection is disposed on a center of the first wiring.

23. (Previously Presented) The method according to claim 13, further comprising the steps of:

(g) disposing a center of the first connection by offsetting it from a center of the first wiring in a direction opposite to the second wiring; and

(h) disposing a projecting portion of the first wiring under the first connection.

24. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

disposing:

(a) a first wiring extending in a first direction;

(b) a connection on the first wiring; and

(c) a terminal on the connection extending in a second direction orthogonal to the first direction and having a surplus portion, the surplus portion projecting from the connection in a direction opposite to the second direction, and

(d) disposing a second wiring in the second direction from the terminal,

wherein the first wiring includes a projecting portion disposed under the connection.

25. (original) A method of manufacturing a semiconductor device, comprising the steps of:

(a) defining a first layout line of a first wiring layer extending in a first direction and a second layout line of a second wiring layer extending in a second direction orthogonal to the first direction;

(b) disposing virtually a first wiring along the first layout line, the first wiring having projecting portions respectively on both sides of an intersecting point of the first and the second layout lines;

(c) disposing a second wiring along the second layout line;

(d) disposing a connection in an overlapped region of patterns of the first and the second wirings; and

(e) defining a pattern of the first wiring with the projecting portions of the first wiring disposed only under the connection.

26. (Previously Presented) A semiconductor device comprising:

(a) a first wiring extending in a first direction;

(b) a second wiring connected to the first wiring through a connection and extending in a second direction orthogonal to the first direction, the second wiring having a surplus portion projecting in a direction opposite to the second direction;

(c) the connection being formed so that a center thereof is offset in the second direction from a center of the first wiring; and

(d) the first wiring having a projecting portion formed under the connection.

27. (Previously Presented) A semiconductor device comprising:

(a) a first wiring and a second wiring extending in a first direction and being adjacent to each other;

(b) a third wiring being connected to the first wiring through a first connection and extending in a second direction orthogonal to the first direction and in opposition to the second wiring, the third wiring having a first surplus portion projecting in the direction of the second wiring from the first connection;

(c) a fourth wiring being connected to the second wiring through a second connection and extending in the second direction and in opposition to the first wiring,

the fourth wiring having a second surplus portion projecting in the direction of the first wiring from the second connection;

(d) the second connection being formed so that a center thereof is offset from a center of the second wiring in a direction opposite to the first wiring; and

(e) the second wiring having a projecting portion formed under the second connection.

28. (original) The semiconductor device according to claim 27, wherein the distance between a center of the first wiring and that of the second wiring is a unit distance in wiring.

29. (original) The semiconductor device according to claim 27, further comprising a fifth wiring formed in parallel with the third wiring.

30. (original) The semiconductor device according to claim 29, wherein the distance between the third and the fifth wirings is smaller than the distance between the first and the second wirings.

31. (original) The semiconductor device according to claim 29, wherein the distance between the first and the second wirings is smaller than a minimum machining size.

32. (original) The semiconductor device according to claim 29, wherein the width of each of the first and the second surplus portions is smaller than the difference (P0-P1) between a distance P1 between a center of the third wiring and that of the fifth wiring and a distance P0 between a center of the first wiring and that of the second wiring, and is larger than one half of the difference between the distances P1 and P0.

33. (Currently Amended) The semiconductor device according to claim 27, wherein the width of each of the first and the second wirings and the width of each of the first and the second connections are ~~almost~~ substantially equal to each other.

34. (original) The semiconductor device according to claim 27, further comprising a MISFET which underlies the first and the second wirings, a gate electrode of the MISFET being disposed in the first direction between the first and the second wirings.

35. (Previously Presented) The semiconductor device according to claim 27, further comprising a MISFET which underlies the first and the second wirings,

wherein the first or the second wiring is connected to a source and a drain, or a gate electrode, of the MISFET.

36. (original) The semiconductor device according to claim 27, wherein a center of the first connection is disposed on a center of the first wiring.

37. (original) The semiconductor device according to claim 27, wherein:

(f) the first connection is formed so that a center thereof is offset from a center of the first wiring in a direction opposite to the second wiring; and

(g) the first wiring has a projecting portion formed under the first connection.

38. (original) A semiconductor device comprising:

(a) a first wiring extending in a first direction and having at least one projecting portion; and

(b) a second wiring connected to the first wiring through a first connection and extending from the first connection in a second direction orthogonal to the first

direction, the second wiring having a first surplus portion projecting from the first connection in a direction opposite to the second direction,

the first connection being formed on the first wiring and the projecting portion thereof.

39. (Currently Amended) A semiconductor device comprising:

(a) a first wiring extending in a first direction and having at least one projecting portion;

(b) a second wiring connected to the first wiring through a first connection formed on the first wiring and extending from the first connection in a second direction orthogonal to the first direction, the second wiring having a first surplus portion projecting from the first connection in a direction opposite to the second direction; and

(c) a third wiring connected to the first wiring through a second connection and extending from the second connection in a second direction orthogonal to the first direction, the third wiring having a second surplus portion projecting from the second connection in a direction opposite to the second direction, ~~the first connection being formed on the first wiring, and~~ the second connection being formed on the first wiring and the projecting portion thereof.

40. (New) The method of manufacturing a semiconductor device according to claim 1, wherein the projecting portion is formed only under the connection.

41. (New) The method of manufacturing a semiconductor device according to claim 2, wherein the projecting portion is formed only under the second connection.

42. (New) The semiconductor device according to claim 26, wherein the projecting portion is formed only under the connection.

43. (New) The semiconductor device according to claim 27, wherein the projecting portion is formed only under the second connection.

44. (New) The semiconductor device according to claim 38, wherein the projecting portion is formed only under the first connection.

45. (New) The method of manufacturing a semiconductor device according to claim 24, wherein the projecting portion is formed only under the connection.

46. (New) The semiconductor device according to claim 39, wherein the projecting portion is formed only under the second connection.